

### REMARKS

The Applicants respectfully request further examination and reconsideration in view of the amendments made above and the comments set forth below. Within the Final Office Action, claims 1-17 have been rejected. Claims 1, 7-8, and 14 have been rejected under 35 U.S.C. § 102(a). Claim 13 has been rejected under 35 U.S.C. §§ 102(b) and 102(e). Claims 2-12, and 15-17 have been rejected under 35 U.S.C. § 103. Claims 1 and 13-17 have been amended, and claims 18-22 have been added. Accordingly, claims 1-22 are pending.

#### **Rejections under 35 U.S.C. § 102(a)**

Within the final Office Action, claims 1, 7-8, and 14 were rejected under 35 U.S.C. § 102(a) as being anticipated by Japanese Patent Number JP2000-106358A, to Yasuda (“Yasuda”). The Applicants respectfully disagree with these rejections.

Yasuda is directed to a system for processing semiconductor wafers. The system comprises a processing tub for plasma etching a semiconductor wafer. [Translation of Yasuda, ¶ 0007] The system is also configured to clean the processing tub and an enclosed wafer using supercritical fluids. [*Id.*, ¶¶ 0026 and 0030] In Figures 1 and 2, cited within the Final Office Action, Yasuda teaches a hydraulic jack 111 coupled to a septum 110. The septum 110 is coupled to a support 117, which in turn is coupled to a maintenance base 101. The maintenance base 101 functions as a wafer platen, supporting the wafer 102 during both wafer processing and tub cleaning. The system also comprises a microwave generator (not shown) coupled to the interior of the processing tub. [*Id.*, ¶ 0018] The microwave generator generates a plasma within the interior of the processing tub, which is used to etch the semiconductor wafer. [*Id.*, ¶ 0025]

As illustrated in Figure 1, during low-pressure processing (e.g., etching) of the wafer 102, neither the maintenance base 101 nor the septum 110 forms a seal with the processing tub. In this way, a flow path is created so that processing gas is pumped through the gas inlet 103, over the wafer 102, and out the exhaust port 106. The maintenance base 101 can be optimally raised to perform dry etching. [*Id.*, ¶ 0024] As illustrated in Figure 2, during high-pressure cleaning of the processing tub, the septum 110—not the maintenance base 101—contacts a corner 191 of the processing tub 100a to form a wafer processing chamber around the wafer. [*Id.*, ¶ 0022] Thus, during high-pressure cleaning, the septum 110 provides a sealing surface to form a chamber. The maintenance base 101 (i.e., wafer platen) does not contact the processing tub to form a high-pressure chamber. The statement within the final Office Action that “Yasuda discloses a high

pressure chamber (Abstract and Fig 1 and 2) . . . comprising . . . a platen for holding semiconductor substrates and a second sealing surface (110)” is incorrect.

Yasuda further teaches a recycle segment comprising a separation tub 119 and a compressor 121. Along the recycle segment, supercritical fluid and polymeric material are transmitted to the separation tub 119, where the temperature and pressure are adjusted so that the supercritical fluid is returned to a gas from which the polymeric material is extracted. The gas is then transmitted to a compressor 121 and on to the processing tub 100a, where it is again returned to a supercritical state. [*Id.*, ¶ 0028] Thus, a supercritical fluid is neither maintained nor circulated along a circulation loop.

The present invention is directed to a high-pressure chamber for processing a semiconductor substrate. The chamber comprises a chamber housing, a platen, and a single mechanical drive mechanism. The chamber housing comprises a first sealing surface. The platen comprises a region for holding the semiconductor substrate and a second sealing surface. The single mechanical drive mechanism has a single pressure source for forming and maintaining a wafer cavity for containing the semiconductor substrate during high pressure processing. The single mechanical drive mechanism couples the platen to the chamber housing such that in operation the single mechanical drive mechanism separates the platen from the chamber housing for loading of the semiconductor substrate and further such that in operation the said single mechanical drive mechanism causes the second sealing surface of the platen and the first sealing surface of the chamber housing to contact, thus forming the wafer cavity and maintaining the wafer cavity during high pressure processing. As described above, Yasuda does not teach a platen having a region for holding a semiconductor substrate and a second sealing surface.

Within the Final Office Action it is stated, “Applicant argues repeatedly that the claims distinguish over Toru Yasuda since the sealing plate is called a septum and not a platen. This argument is not persuasive since (Fig 1-110) clearly shows this to be a platen.” This statement misstates the Applicants’ arguments. What the Applicants argue here and in the Amendment and Response to Office Action Mailed on August 14, 2003, (the August 14<sup>th</sup> Response) is that Yasuda does not disclose a platen that both (1) supports a wafer and (2) provides a sealing surface. The Applicants argue here and in the August 14<sup>th</sup> Response that Yasuda discloses a different structure, one having a platen (or maintenance base) for supporting a wafer and (2) a separate septum for forming a sealing and thus a chamber. The two structures are different and

can be used to perform different tasks. For at least these reasons, claim 1 distinguishes over Yasuda and is allowable.

Claims 7 and 8 depend from claim 1. As described above, claim 1 is allowable over the teachings of Yasuda. Accordingly, claim 7 and 8 are allowable as depending from an allowable base claim.

Claim 14 is directed to a high pressure chamber for processing of a semiconductor substrate. The high pressure chamber comprises a chamber housing, a platen, a single mechanical drive mechanism, a means for sealing, and a means for maintaining a supercritical fluid and circulating the supercritical fluid through a wafer cavity. The platen comprises a region for holding the semiconductor substrate. The single mechanical drive mechanism has a single pressure source for forming and maintaining a wafer cavity for containing the semiconductor substrate during high pressure processing. The single mechanical drive mechanism couples the platen to the chamber housing such that in operation the single mechanical drive mechanism separates the platen from the chamber housing for loading of the semiconductor substrate. The means for sealing is coupled to the chamber housing such that in operation the single pressure source causes the means for sealing, the platen, and the chamber housing to form the wafer cavity and maintain the wafer cavity during high pressure processing. As described above, Yasuda does not teach a platen that both holds a semiconductor substrate and forms a wafer cavity. Nor does Yasuda teach a means for maintaining a supercritical fluid and circulating the supercritical fluid through a wafer cavity. For at least these reasons, claim 14 is allowable over the teachings of Yasuda.

Within the Final Office Action, claim 13 is rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,979,306 to Fujikawa *et al.* ("Fujikawa"). The Applicants respectfully disagree with this conclusion.

Fujikawa discloses a system for reliably sealing a processing chamber. [Fujikawa, Abstract] Referring to Figure 2, Fujikawa discloses shaped parts 6A and 6B, a raising and lowering actuator 11 for moving the shaped parts 6A and 6B together, and a pressure ram 18 for maintaining the shaped parts 6A and 6B together during processing. At column 4, lines 27-41, the invention in Fujikawa is described:

The above-mentioned pressing means is formed of a ram using gas pressure having a pressure medium chamber to which the pressurized gas of the gas introducing means can be introduced, and the pressure receiving area of the ram is set larger than the pressure

receiving area of the processing space. By adapting such a structure, the gas of the same pressure as the gas filled in the high-pressure gas processing space is basically introduced into the gas pressure ram, so that the upper and lower vessel components are regularly kept in the mutually closely fitted state at the parting plane so long as the gas pressure is supplied, and the high-pressure gas within the high-pressure gas processing space can be prevented from being leaked through the parting plane to the outside by the synergistic effect with the sealing effect on the seal ring which is the elastic body.

Referring to Figure 5 of Fujikawa, Fujikawa discloses a system in which a processing gas is pumped by the gas compressor 26 to both the processing space 5 and the gas pressure ram 18 simultaneously. Gas is supplied to the processing space 5 to process a workpiece and gas is supplied to the gas pressure ram 18 to maintain the seal. Configured to use a single source to supply a processing gas and a sealing force, Fujikawa does not teach or suggest using a circulation loop coupled to the supercritical processing module and configured to maintain a supercritical fluid and circulate the supercritical fluid through the workpiece cavity. Indeed, there is no indication of how Fujikawa could be adapted to accomplish this.

Claim 13 is directed to a high pressure chamber for processing a semiconductor substrate. The high pressure chamber comprises a chamber housing comprising a first sealing surface, a platen comprising a second sealing surface and a region for holding the semiconductor substrate, a single mechanical drive mechanism, a mechanical clamp, and a circulation loop. The single mechanical drive mechanism has a single pressure source for forming a wafer cavity for containing the semiconductor substrate. The single mechanical drive mechanism couples the platen to the chamber housing such that in operation the single mechanical drive mechanism separates the platen from the chamber housing for loading the semiconductor substrate and further such that in operation the said single mechanical drive mechanism causes the second sealing surface of the platen and the first sealing surface of the chamber housing to contact, thus forming the wafer cavity. The mechanical clamp is coupled to the chamber housing and the platen such that in operation the mechanical clamp maintains the wafer cavity during high pressure processing. The circulation loop is coupled to the wafer cavity and is configured to maintain a supercritical fluid and circulate the supercritical fluid through the wafer cavity. As described above, Fujikawa does not teach a circulation loop at all, let alone one configured to maintain a supercritical fluid and circulate the supercritical fluid through a wafer cavity. For at least this reason, claim 13 is allowable over the teachings of Fujikawa.

Within the Final Office Action, claim 13 has been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,508,259 to Tseronis *et al.* ("Tseronis"). The Applicants respectfully disagree with this conclusion.

Tseronis discloses an inverted pressure vessel suitable for wafer processing. Figure 3 of Tseronis discloses an inverted pressure vessel comprising a pressure vessel 1, a closing plate 2, an axial lift rod 4 coupled to the closing plate 2, and a lower end lift rod drive 8 coupled to the axial lift rod 4. The closing plate 2 functions as a support for a wafer. [Tseronis, col. 5, lines 6-11] In operation, the lower end lift rod drive 8 lifts the axial lift rod 4 and thus the closing plate against the pressure vessel 1, thereby forming a processing cavity. Tseronis does not teach a spacer. Moreover, Tseronis specifically does not teach any structure for circulating a fluid within a processing cavity. Indeed, at column 5, lines 1-5, Tseronis states, "Not shown are the channels and ports for admitting and removing process fluids from the vessel, and such heaters, internal or external, as may be required for achieving process temperature environments."

As described above, claim 13 is directed to a high pressure chamber for processing a semiconductor substrate. The high pressure chamber comprises a chamber housing comprising a first sealing surface, a platen comprising a second sealing surface and a region for holding the semiconductor substrate, a single mechanical drive mechanism, a mechanical clamp, and a circulation loop. The single mechanical drive mechanism has a single pressure source for forming a wafer cavity for containing the semiconductor substrate. The single mechanical drive mechanism couples the platen to the chamber housing such that in operation the single mechanical drive mechanism separates the platen from the chamber housing for loading the semiconductor substrate and further such that in operation the said single mechanical drive mechanism causes the second sealing surface of the platen and the first sealing surface of the chamber housing to contact, thus forming the wafer cavity. The mechanical clamp is coupled to the chamber housing and the platen such that in operation the mechanical clamp maintains the wafer cavity during high pressure processing. The circulation loop is coupled to the wafer cavity and is configured to maintain a supercritical fluid and circulate the supercritical fluid through the wafer cavity. As described above, Tseronis does not teach a circulation loop at all, let alone one configured to maintain a supercritical fluid and circulate the supercritical fluid through a wafer cavity. For at least this reason, claim 13 is allowable over the teachings of Tseronis.

**Rejections under 35 U.S.C. § 103**

Within the Final Office Action, claims 2-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yasuda in view of U.S. Patent No. 5,798,126 to Fujikawa *et al.* Claims 2-6 all depend from claim 1. As described above, claim 1 is allowable. Accordingly, claims 2-6 are all also allowable as depending from an allowable base claim.

Within the Final Office Action, claim 4-5 and 7-9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yasuda in view of U.S. Patent No. 5,979,306 to Fujikawa *et al.* (Within the Final-Office Action, it is mistakenly stated that these claims are rejected under 35 U.S.C. § 102(b).) Claims 4-5 and 7-9 all depend from claim 1. As described above claim 1 is allowable. Accordingly, claims 4-5 and 7-9 are all also allowable as depending from and allowable base claim.

Within the Final Office Action, claims 10-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yasuda in view of U.S. Patent No. 5,898,727 to Fujikawa *et al.* Claims 10-12 all depend from claim 1. As described above claim 1 is allowable. Accordingly, claims 10-12 are all also allowable as depending from and allowable base claim.

Within the Final Office Action, claims 15-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yasuda in view of U.S. Patent No. 6,077,053 to Fujikawa *et al.* ("Fujikawa II"). The Applicants respectfully disagree with this rejection.

Within the Final Office Action, it is stated that Fujikawa II discloses a "gas compressor using pistons." Nowhere is it stated that Fujikawa II teaches a circulation loop coupled to a wafer cavity and configured to maintain a supercritical fluid and circulate the supercritical fluid through the wafer cavity. Moreover, as described above, Yasuda also does not teach this structure.

Claim 15 is directed to an apparatus for high pressure processing of a semiconductor substrate. The apparatus comprises a pressure chamber frame, a single piston coupled to the pressure chamber frame and comprising a piston body and a piston neck, a sealing plate coupled to the pressure chamber frame, a platen coupled to the piston neck, a top lid coupled to the pressure chamber frame and comprising a second sealing surface, and a circulation loop. The pressure chamber frame and the piston body form a first fluid cavity. The sealing plate in conjunction with the pressure chamber frame, the piston body, and the piston neck forms a second fluid cavity. The platen comprises a region for holding the semiconductor substrate and a first sealing surface. The first sealing surface of the platen and the second sealing surface of the

top lid are configured such that in operation the piston body can be moved using a single pressure within the first fluid cavity so that the first and second sealing surfaces contact to form a wafer cavity and to maintain the wafer cavity during high pressure processing. In further operation the piston body can be moved so that the first and second sealing surfaces do not contact, thereby allowing the semiconductor substrate to be loaded into and unloaded from the pressure chamber frame. The circulation loop is configured to maintain a supercritical fluid and circulate the supercritical fluid through the wafer cavity. As described above, neither Yasuda nor Fujikawa II teaches a circulation loop configured to circulate a supercritical fluid through a wafer cavity, as recited in claim 15. For at least this reason, claim 15 is allowable over Yasuda, Fujikawa II, and their combination.

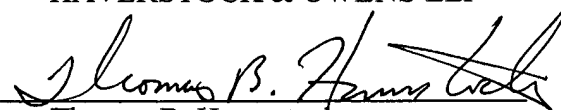
Claims 16 and 17 both depend from claim 15. As described above, claim 15 is allowable over the teachings of Yasuda, Fujikawa II, and their combination. Accordingly, claim 16 and 17 are both allowable as depending on an allowable base claim.

The new claims 18-22 all ultimately depend from claim 1. As discussed above, claim 1 is allowable. Accordingly, claim 18-22 are all allowable as depending from an allowable base claim.

No new matter has been added by the above amendments. For the reasons given above, the Applicants respectfully submit that claims 1-22 are in condition for allowance, and allowance at an early date would be appreciated. If the Examiner has any questions or comments, the Examiner is encouraged to call the undersigned at (408) 530-9700 to discuss them so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,  
HAVERSTOCK & OWENS LLP

Dated: 1-7-04

By:   
Thomas B. Haverstock  
Reg. No.: 32,571

Attorneys for Applicants

**CERTIFICATE OF MAILING (37 CFR § 1.8(a))**

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

HAVERSTOCK & OWENS LLP

Date: 1-7-04 By: 